

## **I. Drawings**

The Examiner approved of the prior correction to the drawings. The Examiner is now requiring corrected drawings. Applicants are filing herewith corrected formal drawings which should overcome all of the Examiner's objections to the drawings. The only changes made to the drawings, other than formalizing them, is to correct a couple of spelling errors in Fig. 21A as shown on the marked-up copy. Hence, it is believed that no new matter is being added. Accordingly, Applicants respectfully request that this objection be withdrawn.

## **II. Claim Rejections - 35 USC §103**

The Examiner continues to have the following rejections under 35 USC §103:

- a. Claims 1 and 25 as being unpatentable over Matsumoto in view of Adan et al. and Shimone;
- b. Claims 3 and 27 as being unpatentable over Matsumoto in view of Adan et al., Shimone and Karauchi et al.; and
- c. Claims 21 and 23 as being unpatentable over Matsumoto in view of Adan et al., Shimone, and Karauchi et al. and further in view of Hioki; and in addition,
- d. Claim 53 as being unpatentable over Matsumoto in view of Adan, Shimone, Karauchi and Takasu.

Each of these rejections is respectfully traversed.

The present invention, as recited in the independent claims, is directed to a semiconductor device comprising a pixel section having a pixel TFT and a driver section comprising a p-channel TFT and an n-channel TFT over a substrate. The pixel TFT is an n-channel TFT and has a LDD region. The p-channel TFT of the driver circuit does not have a LDD region. The n-channel TFT of the driver circuit has a LDD region which partly overlaps a gate electrode.

As explained on pages 3-4 of the specification of the present application, the inventors of the present invention recognized that one of the required characteristics of a pixel TFT is to restrict an OFF current value while required characteristics of TFTs in the driver circuit include withstanding high voltage, a sufficient high ON current value and high operational speed. Hence, in each circuit, the required characteristics of the pixel TFT and the driver TFTs are very different, due to the function of each. Further, as explained in the specification, the inventors recognized that a LDD structure has a high effect for preventing OFF current value, it does not have the effect of releasing the electric field in the proximity of the drain and preventing degradation by hot carrier injection. Additionally, the inventors recognized that while a GOLD structure has a high effect for preventing degradation of ON current value, it does not prevent OFF current value.

Accordingly, the inventors conceived of the claimed invention to improve the operational characteristics and reliability of a semiconductor device and at the same time lower the power consumption, by optimizing the structures of the TFTs employed in various circuits in accordance with the functions of the respective circuits. This is accomplished by utilizing the structure claimed in the present application.

Applicants respectfully submit that none of the cited references disclose or suggest such a structure nor is the combination of the references to arrive at the present invention proper.

In the Final Rejection, the Examiner argues that Matsumoto, Adan and Shimone can be combined to arrive at the semiconductor device claimed in independent Claims 1 and 25. Applicants respectfully disagree.

The Examiner admits that Matsumoto does not disclose the claimed LDD region but argues that it would have been obvious for one skilled in the art at the time of the invention to use the partly overlapping LDD regions of Adan in the device of Matsumoto to increase the breakdown voltage of the transistor as allegedly stated by Matsumoto in col. 2, lns. 17-25.

The Examiner, however, fails to state which TFT of Matsumoto is replaced by the TFT of Adan. Further, neither reference provides any teaching or suggestion of such replacement.

The Court of Appeals for the Federal Circuit has stated that in order to combine references, there must be some motivation, teaching or suggestion in the references to combine them. See, e.g. Ecolchem Inc. v. Southern California Edison, 56 USPQ2D 1065, 1072-1076 (Fed. Cir. 2000). Absent such motivation, teaching or suggestion, the combination of the references is improper. Id. In such a situation, such references can only be combined through improper hindsight reconstruction. Since such motivation, teaching or suggestion is absent with regard to the cited references, the combination of these references is improper.

More specifically, the TFT structure of the claimed device was chosen by the inventors according to the function of the circuit and to overcome the above described problems.

Applicants have reviewed the cited references. It appears that Matsumoto discloses in Fig. 1 a pixel section having a pixel TFT (21) and a driver circuit having an n-channel TFT (22) and a p-channel TFT (23); the pixel TFT (21), the n-channel TFT (22) and the p-channel TFT (23) having the same LDD structure, i.e., each LDD region is not overlapped with each gate electrode. It appears that Adan discloses in Fig. 29 an LDD region (71) that partly overlaps a gate electrode (66). It appears that Shimone discloses in Fig. 3d, a pixel electrode (106) disposed in a pixel section, the pixel electrode being formed over an interlayer insulating film (104) of an organic insulating material, and is connected to the pixel TFT through an opening formed in a protective insulating film (113).

Hence, Applicants can find no teaching or suggestion in the cited references regarding choosing which TFT in Matsumoto is suppose to be replaced by the TFT in Adan, unless one resorts to using the claims of the present application as a guide. However, to do so would be hindsight reconstruction which is improper. Accordingly, the combination of these references is improper, and the rejection based thereon should be withdrawn.

Additionally, Applicants respectfully submit that the Examiner's arguments in support of his rejection are incorrect. In particular, the Examiner states that the feature on which Applicant previously relied (i.e. the p-channel TFT of the driver circuit does not have a LDD region) is not recited in the rejected claims. Applicants disagree. Claim 1, for example, states:

“the p-channel TFT of the driver circuit comprises a channel forming region and a p-type impurity region of a fourth concentration that forms a source region or a drain region and is disposed in contact with the channel forming region;” (emphasis added)

Applicants respectfully submit that one skilled in the art would understand that such claim language indicates that the p-channel TFT does not have a LDD region.

As explained in Amendment A, none of the references disclose or suggest the structure of the claimed device of having a pixel TFT and a driver circuit comprising a p-channel TFT and an n-channel TFT, over a substrate; the pixel TFT having a channel forming region and a LDD region; the n-channel TFT of the driver circuit having a LDD region that partly overlaps a gate electrode; and the p-channel TFT of the driver circuit having a channel forming region and a p-type impurity region that forms a source region or drain region and is disposed in contact with the channel forming region, and not a LDD region.

Therefore, for at least the above-stated reasons, it is respectfully submitted that the claims of the present application are not disclosed or suggested by the cited references but are patentable

thereover. Accordingly, it is requested that they now be allowed, and the §103 rejection over Matsumoto, Adan and Shimone be withdrawn.

Furthermore, for substantially the same reasons, the other rejections under §103 are also deficient, and the claims are patentable over those references.


It is respectfully submitted that the present application is now in a condition for allowance and should be allowed.

Please charge our deposit account 50/1039 for any further fee for this amendment.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

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Marked-up copy of the amendments made herein:

**IN THE DRAWINGS:**

Please amend the drawings as shown in red in the attached figures and substitute the corrected formal drawings for the pending drawings.